

The diagram shows a PLL system with a feedback loop. An input signal  $\Delta f_{RF}$  enters a summing junction (circle). The output of the summing junction is labeled  $f_{IF}$  and is connected to a block labeled  $K_d$  (with a DEMO tap). The output of  $K_d$  is labeled  $SD$  and is connected to a block labeled  $ESTB = FIL$ . The output of  $ESTB = FIL$  is connected to a summing junction (circle) that also receives a feedback signal from a block labeled  $COR$ . The output of this second summing junction is labeled  $f_{VCO}$  and is connected to a block labeled  $K_m$  (with a VCO tap). The output of  $K_m$  is labeled  $V_{mod}$  and is connected to an amplifier block labeled  $AMP$ . The output of  $AMP$  is labeled  $MVB$  and is connected to a summing junction (circle) that also receives a reference signal  $V_{ref}$ . The output of this third summing junction is connected to the  $COR$  block, which completes the feedback loop.

FIG.3

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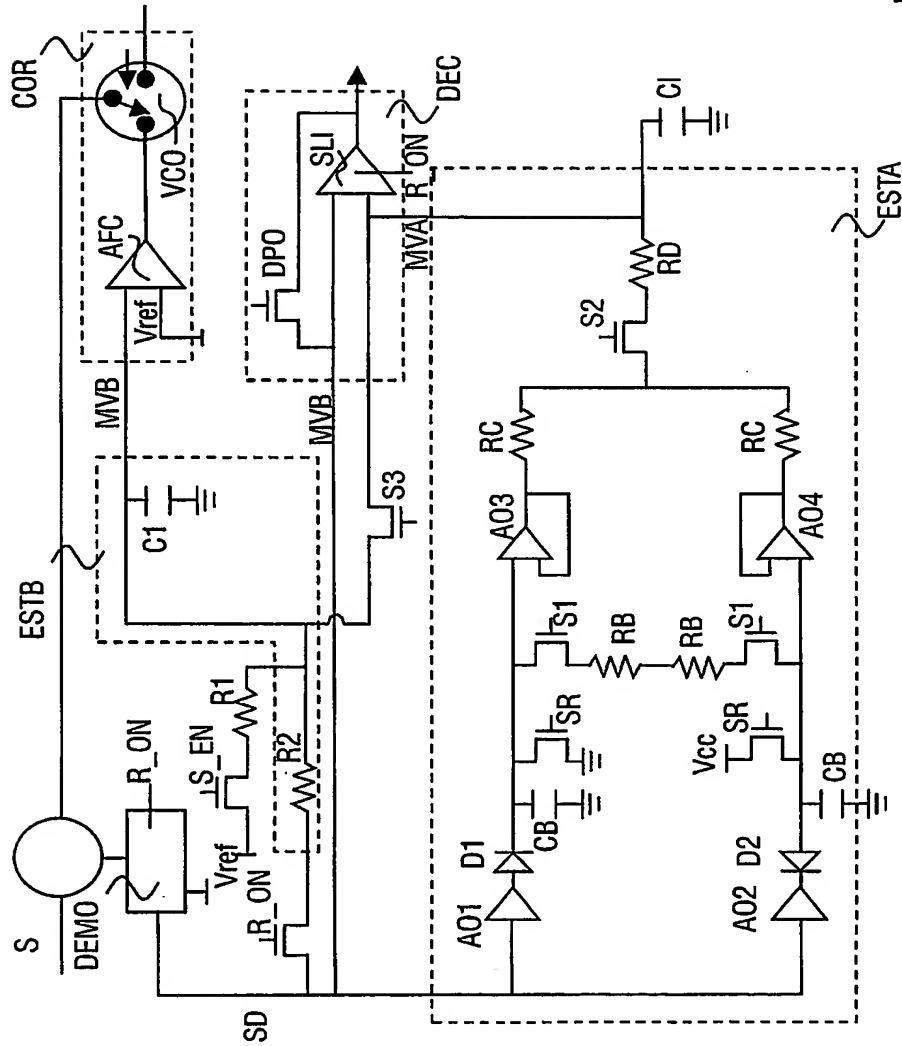


FIG. 4

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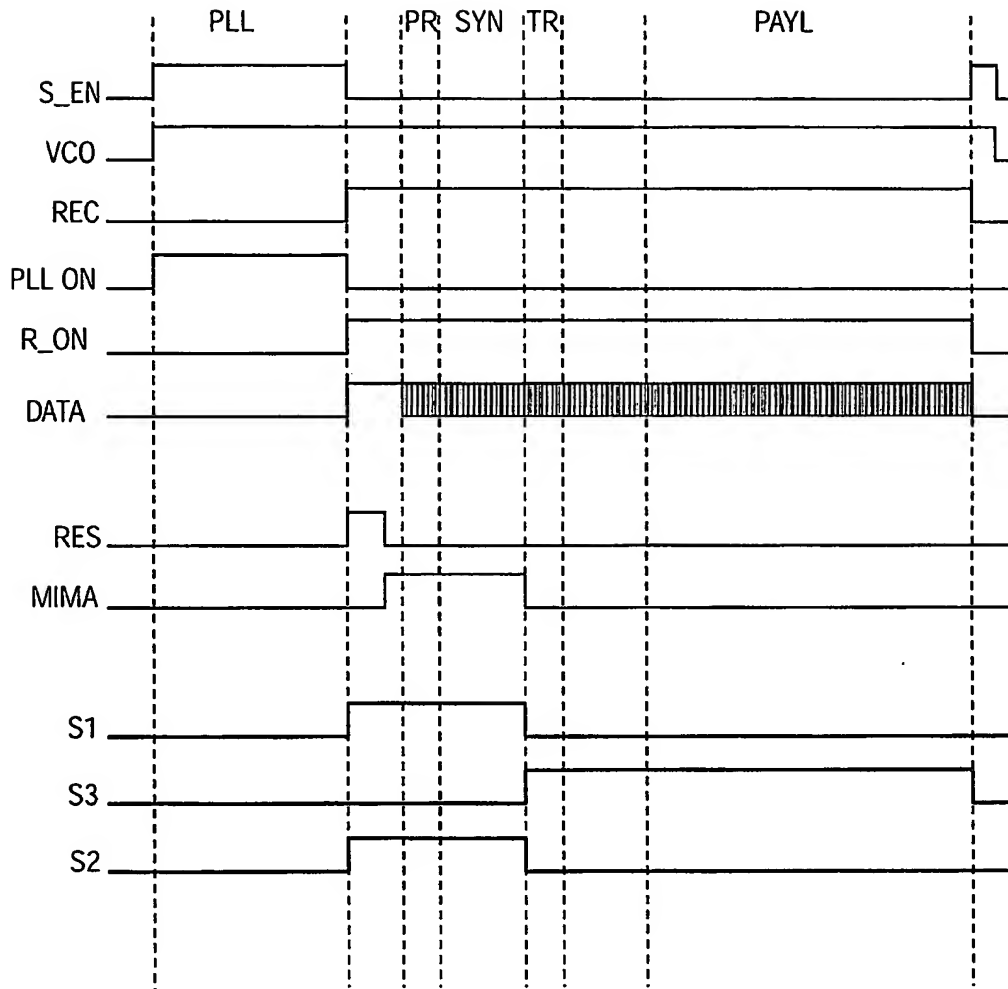


FIG.5

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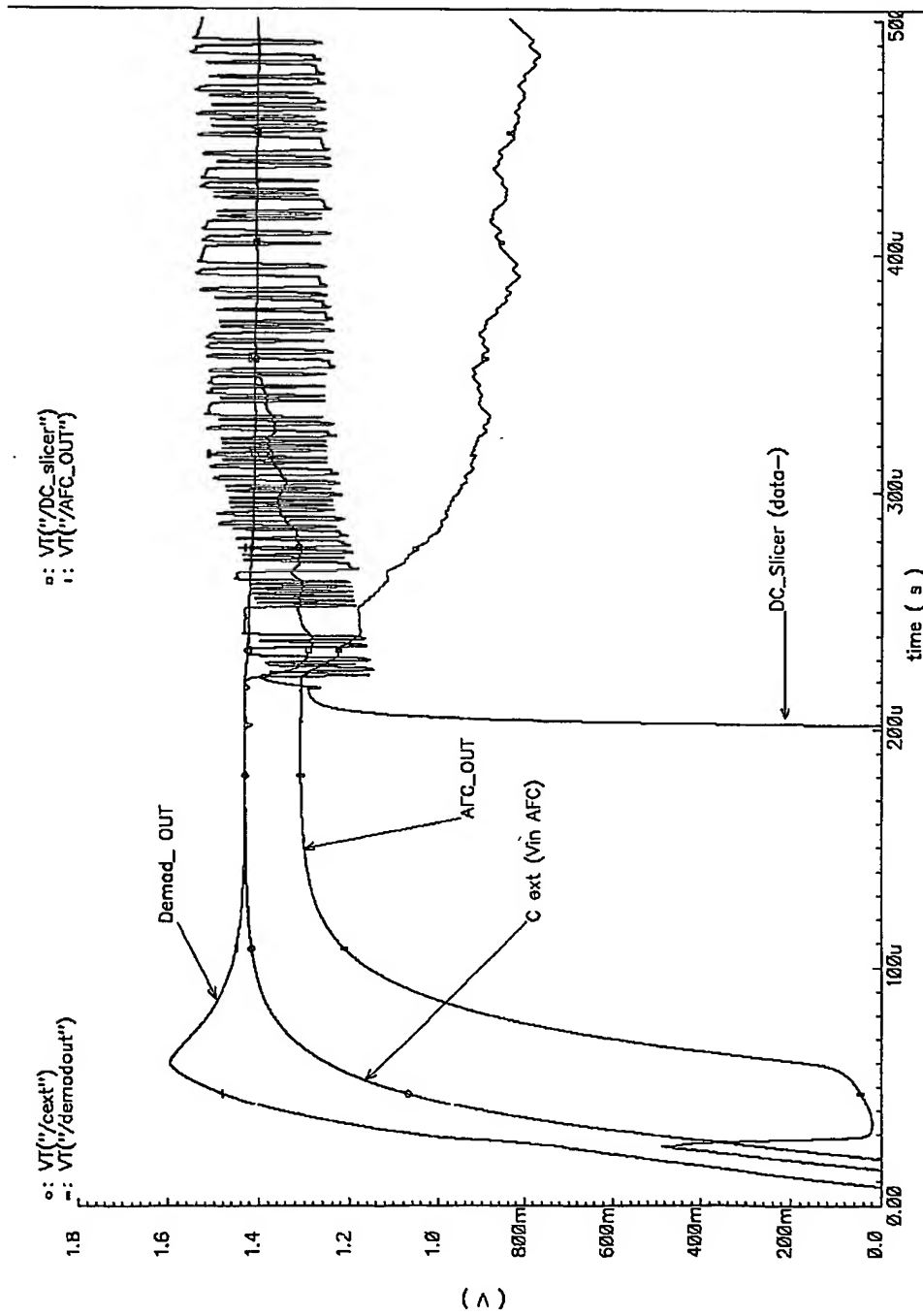


FIG.6